In-situ Formation of Bilayer HfN Gate Insulator Utilizing ECR Plasma Sputtering

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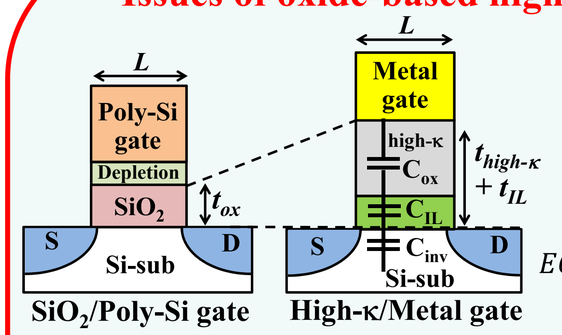
Introduction

Issues of oxide-based high-κ gate insulator



SiO_2/Poly-Si gate High-κ/Metal gate

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{GS}-V_{th})^2$$

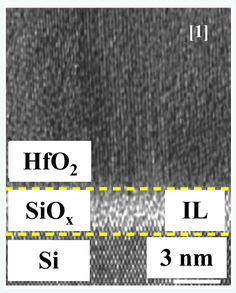
$$C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}} = \frac{\varepsilon_{high-k}}{t_{high-k}}$$

$$EOT = EOT_{IL} + \left(\frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,high-k}}\right)t_{high-k}$$

Gate insulator	κ	E_g (eV)
SiO_2	3.9	8.9
Si_3N_4	7	5.3
Ta_2O_5	25	4.4
HfO_2	25	5.6

MOSFET scaling
- High integration
- High performance
- Low power consumption

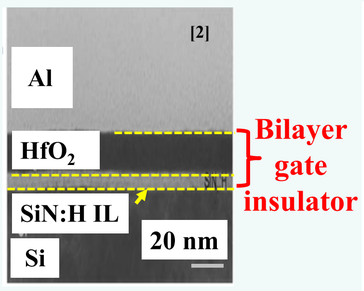
Current issues
- High leakage current (J_g) due to tunneling effects (t_{ox} < 3 nm)



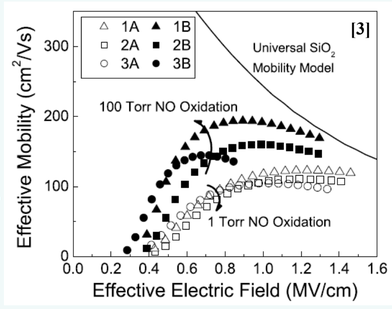
[1] J. Lu, *et. al.*, J. Cryst. Growth, 273, pp. 510-514 (2005).

Relative low-κ interfacial layer (IL) at high-κ/Si interface limits the EOT scaling below 0.5 nm

Bilayer gate insulator with nitride-based IL



[2] H. Garcia, *et. al.*, J. Appl. Phys., 104, p. 094107 (2008).



[3] K. Y. Yang, *et. al.*, Solid-State Electron., 47, pp. 149–153 (2003).

Advantages:
- Free of oxygen atom
- Prevent IL formation
- Higher-κ compared to SiO_2 IL
- EOT scaling

Disadvantages:
- High bulk trapped charges
- High interface trapped charges
- Mobility degradation [3-5]

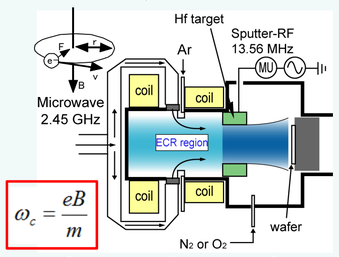
Nitride-based IL with low nitrogen concentration is required at the high-κ/Si interface → HfN_x is the promising candidates [4-7]

[4] H. S. Han and S. Ohmi, IEICE Electronics Exp., 9 (16), pp. 1329-1334 (2012).
[5] N. Atthi, *et. al.*, IEICE Tech. Rep. (SDM), 113 (247), pp. 5-10 (2013).
[6] N. Atthi, *et. al.*, The 61th JSAP spring meeting, 18a-D8-11 (2014).
[7] N. Atthi, *et. al.*, MRS Proceeding., Vol. 1588 (2014).

HfN_x film deposition methods

- CVD methods (ALD and MOCVD) — contamination from precursors
- MBE method — low throughput

Electron-cyclotron-resonance (ECR) plasma sputtering

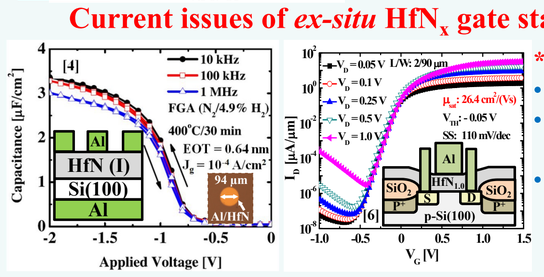


$$\omega_c = \frac{eB}{m}$$

Advantages:
- In-situ process
- Low-surface damage
- Good uniformity

Main process parameters:
- Gas pressure (gas flow ratio)
- RF/μ-wave power

Current issues of *ex-situ* HfN_x gate stack structures



* Low interface quality
- EOT > 0.5 nm
- Oxygen remains (O ~ 5.0%)
- Mobility degradation (μ_{sat} = 26.4 cm²/(Vs))

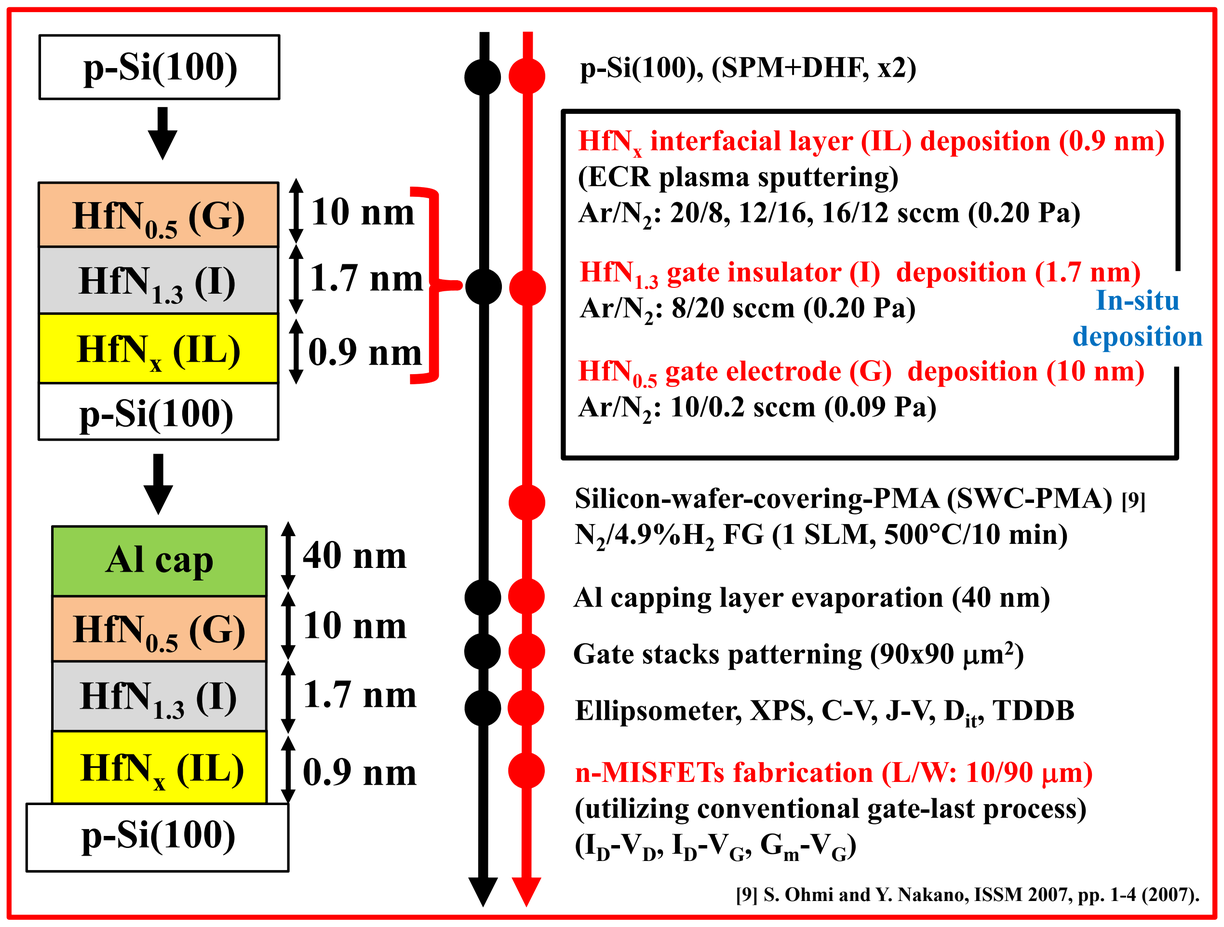
Utilizing HfN_x gate stacks with *in-situ* deposited by ECR plasma sputtering → No contamination and oxidation at the interfaces [8]

[8] N. Atthi and S. Ohmi, The 62nd JSAP Spring Meeting, 13a-A24-12, (2015).

Objectives

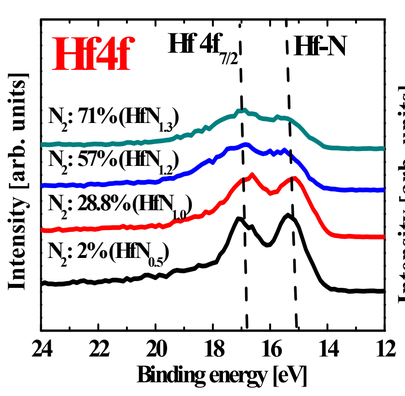
Investigation the effects of *in-situ* formation of bilayer HfN gate insulator utilizing ECR plasma sputtering on the electrical properties and reliability of HfN_x gate stack structures

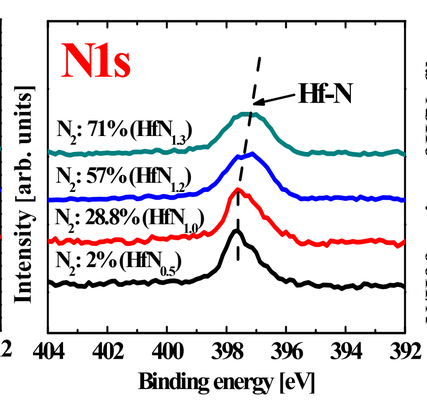
Experimental Procedure

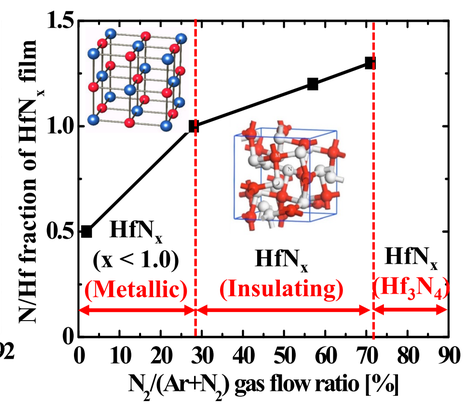


[9] S. Ohmi and Y. Nakano, ISSM 2007, pp. 1-4 (2007).

Stoichiometry of HfN_x films

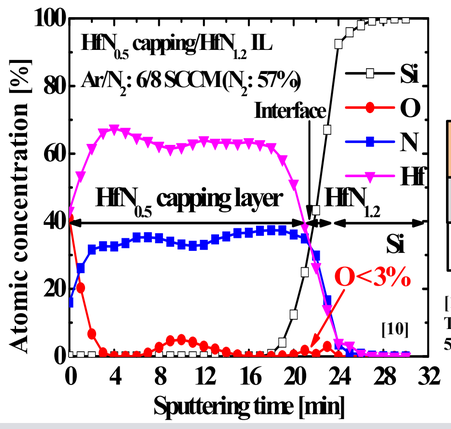


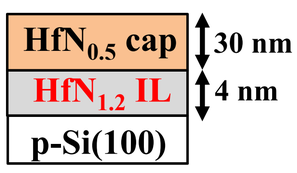




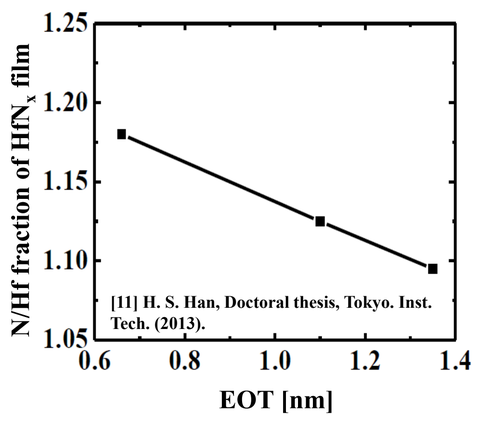
Hf4f spectra of insulating-phase $HfN_{1.3}$ film shows higher binding energy than metallic-phase $HfN_{0.5}$ film, which attributed to the higher concentration of nitrogen in $HfN_{1.3}$ film.

HfN_x film can be changed from metallic-phase to insulating-phase with increasing the nitrogen concentration.





[10] N. Atthi and S. Ohmi, IEICE Tech. Rep. (SDM), 115 (280), pp. 57-62 (2015).



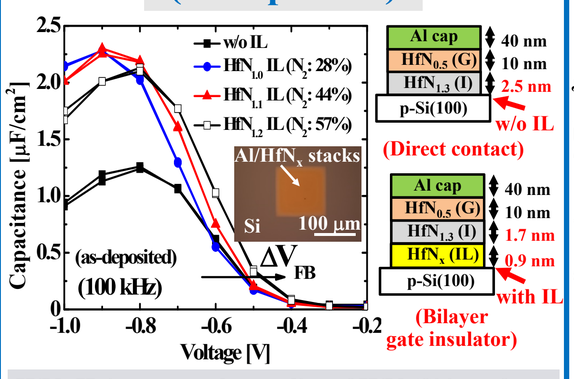
[11] H. S. Han, Doctoral thesis, Tokyo. Inst. Tech. (2013).

In-situ deposition process can suppress the oxygen content at the HfN_x/Si interface below 3.0%

High nitrogen concentration (N/Hf ratio) of HfN_x gate insulator is required for EOT scaling below 0.5 nm

Bilayer HfN_x gate insulator MIS-diode characteristics

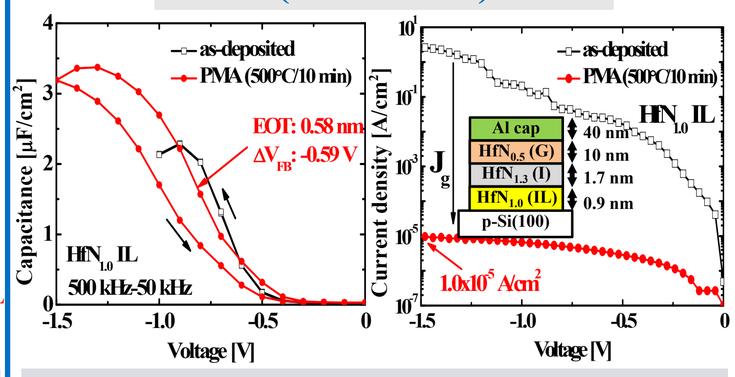
(as-deposited)



HfN_x IL improves the quality of HfN_x/Si interfaces
Large amount of N in $HfN_{1.2}$ IL → high D_{it} and J_g

HfN_x film with N_2 flow ratio below 57%, especially $HfN_{1.1}$ film is suitable for IL

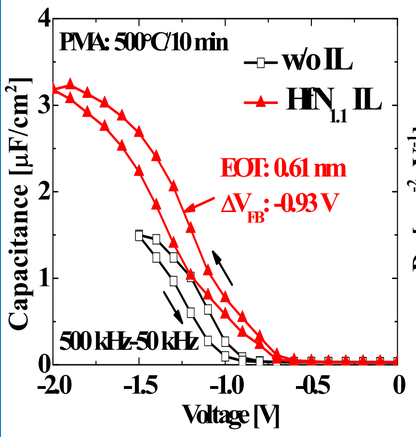
(SWC-PMA)

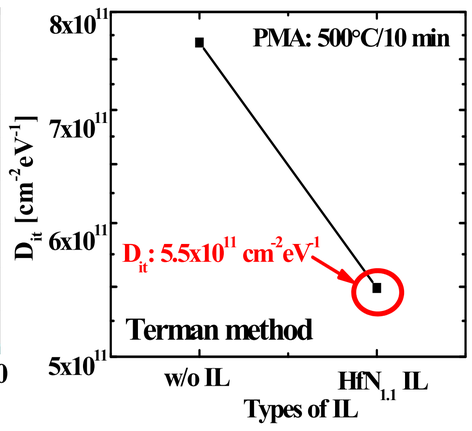


J_g was well suppressed by PMA process. Large hysteresis in C-V curves might due to the PMA condition was not suitable and leads to remain trapped charges in HfN_x gate stacks.

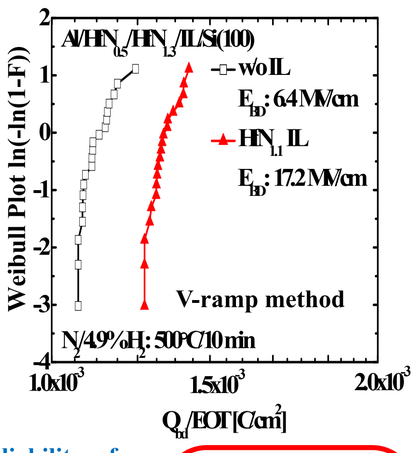
PMA condition should be further optimized

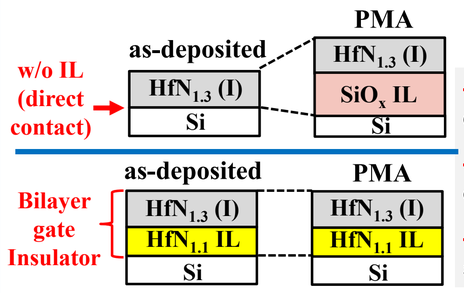
Dependence on N concentration in HfN_x IL





TDDB characteristics

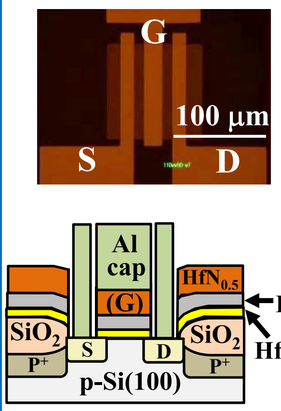


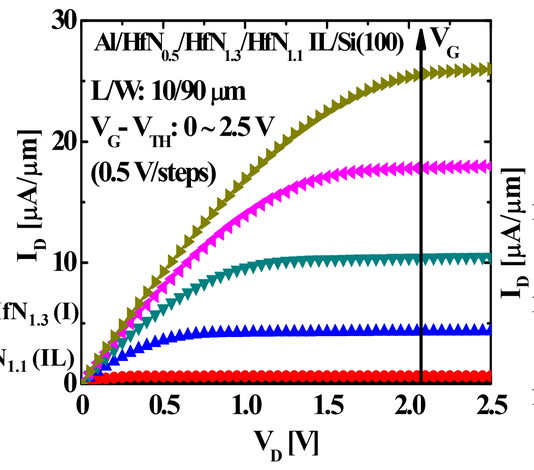


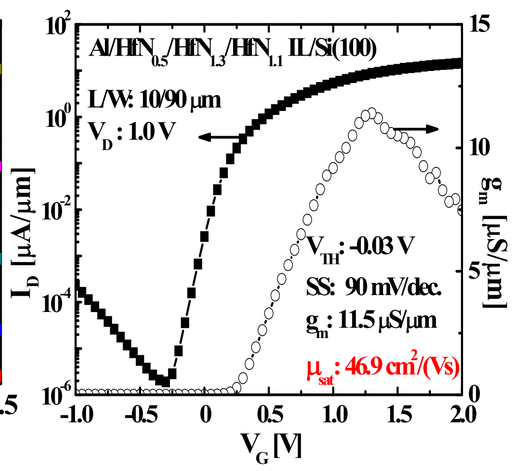
Superior electrical properties and reliability of bilayer HfN_x gate insulator were obtained due to
- $HfN_{1.1}$ IL suppression of the formation of IL during the PMA process.
- ΔV_{FB} behavior is due to negative fixed charges causes by N incorporation.
- PMA process suppressed Si-dangling bond and improved the quality of HfN_x gate stacks.

$HfN_{1.1}$ IL with PMA
- EOT: 0.61 nm
- ΔV_{FB}: -0.93 V
- J_g (@V_{FB} – 1V): 5.5x10⁻³ A/cm²
- D_{it}: 5.5x10¹¹ cm⁻²eV⁻¹
- E_{BD}: 17.2 MV/cm

Bilayer HfN_x gate insulator n-MISFETs characteristics







By using *in-situ* bilayer HfN_x gate insulator annealed in N_2/4.9%H_2 forming-gas (FG) ambient at 500°C/10 min, μ_{sat} of 46.9 cm²/(Vs) was obtained → The increasing mobility is probably due to the improvement of the interface properties by using bilayer HfN_x gate insulator

Conclusions

We investigated the *in-situ* formation of bilayer HfN gate insulator utilizing ECR plasma sputtering for the first time. The bilayer HfN gate insulator shows significantly improved the interface qualities, which leads to the improvement of electrical properties and reliability of HfN_x gate stack structures.

Acknowledgements

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